Digital logic families

Digital logic has evolved over the years and this process has led to the development of a variety of families of digital logic integrated circuits. Each family has its own advantages and limitations. This document describes the main logic families and their characteristics. Among the technologies discussed here are DL, RTL, DTL, ECL, TTL, CMOS and BiCMOS. All of these technologies were developed in the 1950s/1960s and evolved over time. Some of these are still in use today.

Diode Logic (DL)

Diode Logic (DL) is the most primitive of all the digital logic families. It is extremely simple and inexpensive because it only uses passive components. In fact, it combines diodes and resistors so sometimes it is known as Diode-Resistor Logic (DRL).

Since DL does not use active components such as transistors, it does not provide amplification and therefore inversion is not available. For this reason, DL only provides AND and OR functions.

Lack of amplification leads to signal degradation. This is due to the fact there is a voltage drop across diodes and to the fact that when diodes conduct, a voltage divider develops with the inputs.

DL is an obsolete family, primarily due to its limitations in terms of inversion and degradation.
The circuit performs the correct logic but the voltage drop across the diode produces a considerably lower high output voltage (4.2321V).
VBOFFTIME = 200nS
ONTIME = 200nS
DELAY = 0
STARTVAL = 1
OPPVAL = 0

VBOFFTIME = 100nS
ONTIME = 100nS
DELAY = 0
STARTVAL = 1
OPPVAL = 0

D1  1N4376
1   2

D2  1N4376
1   2

DL implementation of the AND function

Waveforms for the AND function

The circuit performs the correct logic but the voltage drop across the diode produces a considerably higher low output voltage (767mV).
Resistor-Transistor Logic (RTL)

Resistor-Transistor Logic (RTL) was invented around 1956. This type of technology, unlike DL, uses active devices such as transistors and therefore can provide inversion. The voltage range goes from 0V for low (0) to 3.5V for high (1). RTL is very inefficient because it dissipates a great amount of power through heat.

RTL has two variants that attempt to improve some of its aspects:

1. When inputs are directly connected to the gate of the BJT, in order to save space and reduce fabrication costs, RTL is known as Direct-Coupled Transistor Logic (DCTL).

2. When capacitors are placed in parallel with input resistors, to speed up operation, RTL is known as Resistor-Capacitor Transistor Logic (RCTL).

Fairchild Semiconductor introduced the first generation of RTL monolithic integrated circuits in either 1962 or 1963. RTL is an obsolete digital logic family.
RTL implementation of the NOT function

Waveforms for the NOT function

This circuit is nothing more than a common-emitter amplifier.
The NOR function can be implemented by the circuit shown above which consists of parallel inputs, a single BJT and two separate power supplies.

Waveforms for the NOR function
RTL implementation of the NOR function (AGC)

The NOR function can be implemented by the circuit shown above. Compared to the previous, this one has only one power supply but it has one BJT per input. The inputs are now isolated, an advantage over the previous circuit.

This solution has been used in 1962 for the Apollo Guidance Computer which, during the Apollo Project, allowed astronauts to land on the Moon.
The NAND function is implemented by the circuit shown above which consists of two parallel inputs, two stacked BJTs and a single power supply.
Waveforms for the NAND function
Diode-Transistor Logic (DTL)

Diode-Transistor Logic (DTL) was invented in the 1950s. It is a major improvement over DL and RTL because it eliminates signal degradation and reduces power dissipation by means of a transistor which restores digital values and a set of input diodes which replace input resistors.

DTL has two variants that attempt to improve some of its aspects:

1. When a capacitor is placed in parallel with the base resistor and an inductor is placed in series with the collector resistor, DTL is known as Complemented Transistor Diode Logic (CTDL).

2. When a Zener diode and a single power supply are connected to the base of the transistor, DTL is known as High-Threshold Logic (HTL).

Signetics introduced the first generation of DTL monolithic integrated circuits in 1962.

DTL was used in the IBM 1401 decimal computer that was delivered in 1959.
DTL implementation of the NOT function

Waveforms for the NOT function
The NOR function can be implemented by the circuit shown above. R₃ is in the circuit to limit excess current from entering the base of the transistor but slows down the switching of the circuit. For this reason the NAND circuit is faster than this NOR circuit.
The NOR function can also be implemented by the circuit shown above. Essentially, this solution is a combination of two inverters. The one on the left is the mirror image of the one of the right. R2 is the common collector resistor. This NOR circuit is faster than the previous one.

By comparing the waveforms for the two NOR circuits, it should be clear that the transition from 00 to 01 is much faster in the second NOR implementation. Eliminating the base resistor speeds up the circuit considerably.
The NAND function is implemented by the circuit shown above. D₁ avoids the situation where one of the inputs is 0 and a sufficient voltage builds at the base of the transistor to turn into conduction.

Waveforms for the NAND function
Emitter-Coupled Logic (ECL)

Emitter-Coupled Logic (ECL) was invented in 1956 by Hannon S. Yourke at IBM. By using a differential amplifier, along with a specific range of input voltages, it is possible to overdrive BJTs so they never enter the saturation region. This type of situation allows extremely high speeds because overdriving avoids the diffusion time that affects the transistor when it transitions from the saturation region to the active region. ECL is fast but it requires a substantial amount of power which in turn produces high heat dissipation. In ECL technology, input impedance is high and output impedance is low. ECL uses only NPN transistors.

ECL was originally known as Current-Steering Logic (CSL) because current can be steered to one side of the differential amplifier while the other side is practically shut off (typical feature of differential amplifiers). ECL is also known as Current-Mode Logic (CML) or Current-Switch Emitter-Follower logic (CSEF).

When MOSFETs replace BJTs, ECL technology is known as Source-Coupled FET Logic (SCFL).

Motorola introduced the first generation of ECL monolithic integrated circuits in 1962 and called it MECL I. Since then, ECL has been on the market and it's still used today.

![Circuit schematic for the MECL 10K by Motorola](image-url)
The circuit shown on the previous page can be divided into three sections: *input*, *compensation* and *output*.

The **input section** has two inputs that are placed in parallel ($V_A$ and $V_B$). The input range has an excursion of less than 1 V. It varies between –1.75V and –1.6V for a low signal (0) and between –0.9V and –0.75V for a high signal (1).

The core of the circuit is the differential amplifier formed by Q1, Q2 and Q3. With a 0 or a 1 at the input, as previously explained, the differential amplifier is overdriven. One side is on and the other is off (one transistor draws all the current and starves the other transistor). The active side (Q1, Q2 or Q3) acts as a *common-emitter stage with emitter degeneration* which provides feedback and therefore additional stability.

R6 acts as a current source that sinks the current from the active branch of the differential amplifier.

The **compensation section**, formed by Q4, R7, R3, D1, D2 and R8, provides temperature and voltage compensation. Essentially, it interfaces input and output stages and locks the circuit in the desired voltage/current range.

The **output section** is formed by Q5 and Q6.

The upper power supply $V_{CC}$ is set to 0V. This is done to avoid variations in voltage from $V_{CC}$ (making it a ground is to set a stable point for the circuit). The lower power supply $V_{EE}$ is –5.2V.

ECL can only provide the OR and NOR functions.

ECL has two variants that attempt to improve some of its aspects:

1. When $V_{CC}$=5V and $V_{EE}$=0V, ECL is known as Positive Emitter-Coupled Logic (PECL). For both inputs and outputs, low logic (0) corresponds to 3.4V and high logic (1) corresponds to 4.2V.
2. When $V_{CC}$ is reduced to 3.3V, in order to reduce power, ECL is known as Low-Voltage Positive Emitter-Coupled Logic (LVPECL). For output voltages, low logic (0) corresponds to 1.6V and high logic (1) corresponds to 2.4V.

ECL was used in the IBM 7030 “Stretch” supercomputer that was delivered in 1961.
Transistor-Transistor Logic (TTL)

Transistor-Transistor Logic (TTL) was invented in 1961 by James L. Buie at TRW. In an attempt to reduce the space utilized on a chip, TTL replaced DTL’s diodes with multiple-emitter transistors. The result was a higher level of integration. TTL is also faster than DTL because it discharges the BE junction of the output transistor more quickly.

Standard TTL chips works with a 5V power supply. For the inputs, the low logic signal (0) should be between 0V and 0.8V and the high logic signal (1) should be between 2V and 5V. For the outputs, the low logic signal (0) stays between 0V and 0.5V the high logic signal (1) corresponds to values between 2.7V and 5V.

Sylvania introduced the first generation of TTL monolithic integrated circuits in 1963. Since then, TTL has evolved and newer generations have been designed to speed up the technology as well as to reduce power consumption.

From 1964 to 2004, different generations of TTL technologies have been invented: L (low-power) and H (high-speed) came in 1964, S (Schottky) in 1969, LS (low-power Schottky) and ALS (advanced low-power Schottky) in 1976\(^1\), F (fast) in 1979, AS (advanced Schottky) in 1980\(^1\) and G in 2004\(^1\).

TTL has been on the market for a long time. It was assigned the 5400, 6400 and 7400 codes. Texas Instruments invented the 5400 line for military applications. The 7400 family was designed for the regular market and became very popular, particularly in the 70s and the 80s, at least until the advent of Very-Large Scale Integrated (VLSI) circuits. The 6400 series did not have a great success and it was a transitional series between 5400 and 7400 in terms of temperature ranges.

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\(^1\) According to Wikipedia, ALS was born either in 1976, 1980 or 1985 and AS was born either in 1980 or 1985.
The NOT function is implemented by the circuit shown above.

This circuit is very similar to its DTL counterpart. Notice that the two diodes are replaced by an NPN transistor in the np/pn sequence.
The NOR function is implemented by the circuit shown above.

This circuit is very similar to its DTL counterpart (diodes are replaced by transistors).
The NAND function is implemented by the circuit shown above.

When the output of the circuit goes to logic 1, the chip offers high resistance at the collector of Q3 and this is undesirable because this situation lowers the fanout (the ability to connect many gates at the output without overloading the circuit). To overcome this deficiency, the *totem-pole* was invented. Although the solution is not optimal, the output is not symmetrical, it is a reasonable way to go about the high resistance problem.

The totem-pole consists of a few additional components: 2 resistors (R3 and R4), 2 transistors (Q4 and Q5) and a diode (D1). The totem-pole is added to the right of what looks like a two-input inverter and it helps to overcome the high output resistance previously mentioned.
Waveforms for the NAND function
Complementary Metal–Oxide Semiconductor (CMOS)

Complementary Metal–Oxide Semiconductor (CMOS) was invented in 1963 by Frank Wanlass at Fairchild semiconductor. This type of technology introduced a new design approach that completely revolutionized the electronics industry: n and p transistors are dual to each other and that they can be combined to provide logic by reducing power consumption (as opposed to previous technologies where only one type of transistor was used).

When compared to older technologies, CMOS drastically reduces power consumption and heat dissipation. CMOS, in fact, consumes power only during changes between logic states, thus only when both transistors are simultaneously active and conduct current. Power dissipated is a function of four variables and it’s described by

\[ P = \alpha CV^2 f \]

where \( \alpha \) is the so-called activity factor, C is capacitance, V is voltage and f is frequency (the activity factor is a number between 0 and 1 that describes how busy is a CMOS device).

CMOS technology became the leading technology for VLSI circuits because it could be highly integrated. As a result, microprocessors and microcontrollers are now made of CMOS devices.

CMOS devices have speed limitations due to internal capacitance which slows down their operation.

CMOS is sensitive to electrostatic discharge or ESD so when handling CMOS devices, additional care needs to be used to avoid damage.

CMOS can operate at different power supply voltages ranging from 3V to 15V. Just like TTL, which became popular with the 7400 family, CMOS has become famous with the 4000 family.

RCA introduced the first generation of CMOS monolithic integrated circuits either in 1968 or in 1970.
Acceptable CMOS gate input signal levels

High

15 V

11 V

Low

4 V

0 V

Acceptable CMOS gate output signal levels

High

15 V

14.95 V

V_{dd} = 15 V

Low

0.05 V

0 V
Static circuits

Static circuits do not use any external clock.

The NOT function is implemented by the circuit shown above. This circuit shows the symmetry and the duality of CMOS technology. The two transistors are complementary and they are mirror images of each other.

The transistors are modeled with the following parameters:

\[ W_p = 100\mu, \ L_p = 2\mu, \ V_{tpo} = -0.7V, \ C_{bpo} = 2.293pF, \ C_{gspo} = 818.1pF, \ C_{gdpo} = 511.3pF \]
\[ W_n = 100\mu, \ L_n = 2\mu, \ V_{tno} = +0.7V, \ C_{bno} = 4.368pF, \ C_{gsno} = 1.329pF, \ C_{gdno} = 496pF \]
The NOR function is implemented by the circuit shown above. This circuit shows the duality of CMOS technology. N transistors are complementary to P transistors (N in parallel and P in series). For static CMOS circuits, for n NMOS transistors, there is an equal number of PMOS transistors.

The transistors are modeled with the following parameters:

\[ W_p=100\mu, \, L_p=2\mu, \, V_{tpo}=-0.7V, \, C_{bdp}=2.293\text{pF}, \, C_{gspo}=818.1\text{pF}, \, C_{gdpo}=511.3\text{pF} \]

\[ W_n=100\mu, \, L_n=2\mu, \, V_{tno}=+0.7V, \, C_{bdn}=4.368\text{pF}, \, C_{gsno}=1.329\text{pF}, \, C_{gdno}=496\text{pF} \]
Static CMOS implementation of the NAND function

The NAND function is implemented by the circuit shown above. This circuit shows the duality of CMOS technology. N transistors are complementary to P transistors (N in series and P in parallel). For static CMOS circuits, for n NMOS transistors, there is an equal number of PMOS transistors.

Waveforms for the NAND function

The transistors are modeled with the following parameters:

- \( W_p=100\mu \), \( L_p=2\mu \), \( V_{tpo}=-0.7V \), \( C_{bdp}=2.293pF \), \( C_{gsno}=818.1pF \), \( C_{gdno}=511.3pF \)
- \( W_n=100\mu \), \( L_n=2\mu \), \( V_{tno}=+0.7V \), \( C_{bdn}=4.368pF \), \( C_{gsno}=1.329pF \), \( C_{gdno}=496pF \)
Complementary Pass-Transistor Logic (CPL) is a CMOS subclass that uses NMOS transistors to provide the logic. It’s generally faster than standard CMOS circuits because eliminating PMOS transistors leads to a reduction in capacitance within the circuit. CPL needs complements of all inputs and provides complements of the implemented functions.

The transistors are modeled with the following parameters:

\[
W_p = 2 \mu, \quad L_p = 100n, \quad V_{tpo} = -0.3V, \quad C_{bdp} = 899.2fF, \quad C_{gsdp} = 2.288fF, \quad C_{gdpo} = 138.5fF
\]

\[
W_n = 100m, \quad L_n = 100n, \quad V_{tno} = +0.3V, \quad C_{bdn} = 118fF, \quad C_{gsno} = 1.885fF, \quad C_{gdno} = 7.564fF
\]
Cascode Voltage Switch Logic (CVSL) is a CMOS subclass that uses NMOS transistors to provide the logic. It’s generally faster than standard CMOS circuits because eliminating PMOS transistors leads to a reduction in capacitance within the circuit. CVSL needs complements of all inputs and provides complements of the implemented functions.

Static CVSL implementation of NOR/OR functions

Waveforms for the NOR/OR functions

The transistors are modeled with the following parameters:

- \( W_p=10 \mu \text{m}, L_p=1 \mu \text{m}, V_{tpo}=-0.5 \text{V}, C_{bdp}=324.9 \text{fF}, C_{gsno}=2.397 \text{fF}, C_{gdno}=306.4 \text{fF} \)
- \( W_n=1 \text{m}, L_n=1 \mu \text{m}, V_{tno}=+0.5 \text{V}, C_{bdn}=377.8 \text{fF}, C_{gsno}=739.4 \text{fF}, C_{gdno}=82.14 \text{fF} \)
Static CVSL implementation of NAND/AND functions

Waveforms for the NAND/AND functions

The transistors are modeled with the following parameters:

\( W_p = 10\mu \text{m}, \quad L_p = 1\mu \text{m}, \quad V_{t_p} = -0.5V, \quad C_{dp} = 324.9fF, \quad C_{sp} = 2.397fF, \quad C_{dpo} = 306.4fF \)

\( W_n = 1m, \quad L_n = 1\mu \text{m}, \quad V_{t_n} = +0.5V, \quad C_{dn} = 377.8fF, \quad C_{sno} = 739.4fF, \quad C_{dno} = 82.14fF \)
Dynamic circuits

Dynamic circuits use external clocks.

Dynamic CPL implementation of the NOR/OR function

Waveforms for the NOR/OR functions

The transistors are modeled with the following parameters:

\[ W_p = 2\mu, \quad L_p = 100n, \quad V_{t_p} = -0.3V, \quad C_{bd_p} = 899.2fF, \quad C_{gs_p} = 2.288fF, \quad C_{gd_p} = 138.5fF \]

\[ W_n = 100m, \quad L_n = 100n, \quad V_{t_n} = +0.3V, \quad C_{bd_n} = 118fF, \quad C_{gs_n} = 1.885fF, \quad C_{gd_n} = 7.564fF \]

The PMOS transistor (pr0B) is called the weak-keeper. It is small in size and it helps to avoid output voltage degradation.
Dynamic CVSL implementation of NOR/OR functions

Waveforms for the NOR/OR functions

The transistors are modeled with the following parameters:

- $W_p=500\mu m$, $L_p=100n$, $V_{tpo}=-0.5V$, $C_{bdp}=324.9pF$, $C_{gsdo}=2.397pF$, $C_{gdpo}=306.4pF$
- $W_n=1m$, $L_n=1\mu m$, $V_{tno}=+0.5V$, $C_{bdr}=377.8fF$, $C_{gsno}=739.4fF$, $C_{gdno}=82.14fF$
Dynamic CVSL implementation of NAND/AND functions

Waveforms for the NAND/AND functions

The transistors are modeled with the following parameters:

\[ W_p=500\mu, L_p=100n, V_{tpo}=-0.5V, C_{bpo}=324.9pF, C_{gspo}=2.397pF, C_{gdpo}=306.4pF \]
\[ W_n=1m, L_n=1\mu, V_{tno}=+0.5V, C_{bdn}=377.8fF, C_{gsno}=739.4fF, C_{gdno}=82.14pF \]
Domino Logic is a CMOS subclass that uses NMOS transistors to provide the logic. It's generally faster than standard CMOS circuits because eliminating PMOS transistors leads to a reduction in capacitance within the circuit. When the clock is 0 (precharge phase), pr0 charges the node below it to 1. When the clock is 1 (evaluation phase), NMOS transistors provide the logic to the output. The clock signal can also be split and two separate clocks can be supplied to the circuit. Sometimes, these two signals overlap. Domino does not need complements of all inputs.

Domino implementation of the OR function

Waveforms for the OR function

The transistors are modeled with the following parameters:

\[
\begin{align*}
W_p &= 1 \text{m}, \quad L_p = 1 \mu, \quad V_{tpo} = -0.3V, \quad C_{bdp} = 2.293fF, \quad C_{gsno} = 818.1fF, \quad C_{gdpo} = 5.113fF \\
W_n &= 1 \text{m}, \quad L_n = 1 \mu, \quad V_{tno} = +0.3V, \quad C_{bdr}= 4.368fF, \quad C_{gsno} = 1.329fF, \quad C_{gdno} = 4.96fF
\end{align*}
\]

PMOS transistor IRFU9010 acts as a weak-keeper. It is small in size (1/10 of NMOS) and it helps to avoid output voltage degradation.
The transistors are modeled with the following parameters:

\[
\begin{align*}
W_p &= 1\, \text{m}, \quad L_p = 1\, \mu, \quad V_{tpo} = -0.3\, \text{V}, \quad C_{bdp} = 2.293\, \text{fF}, \quad C_{gsno} = 818.1\, \text{fF}, \quad C_{gdno} = 5.113\, \text{fF} \\
W_n &= 1\, \text{m}, \quad L_n = 1\, \mu, \quad V_{tno} = +0.3\, \text{V}, \quad C_{bdn} = 4.368\, \text{fF}, \quad C_{gsno} = 1.329\, \text{fF}, \quad C_{gdno} = 4.96\, \text{fF}
\end{align*}
\]

PMOS transistor IRFF9233 acts as a weak-keeper. It is small in size (1/10 of NMOS) and it helps to avoid output voltage degradation.
**Bipolar-CMOS (BiCMOS)**

Bipolar-CMOS (BiCMOS) was invented in 1969. This type of technology is hybrid in nature because it combines bipolar transistors (BJTs) to field effect transistors (MOSFETs) in order to combine the advantages of both devices.

The BJT has low output resistance, high switching speed and high voltage gain. The MOSFET exhibits high input impedance and low power consumption.

BiCMOS has also some disadvantages that prevent this type of technology from becoming popular. Since BJTs are much bigger than CMOS circuits, it is virtually impossible to fabricate integrated circuits at competitive prices because their fabrication would require additional steps and therefore additional costs. BiCMOS has also higher power consumption than CMOS so BiCMOS is not particularly appealing when saving energy is an issue.

The circuit can be divided in two stages: the input stage consists of CMOS transistors whereas the output stage is made by BJT transistors.
BiCMOS implementation of the NOT function

Waveforms for the NOT function

The transistors are modeled with the following parameters:

\[ W_p = 1\mu, \quad L_p = 45n, \quad V_{tpo} = -0.5V, \quad C_{bdp} = 2.293fF, \quad C_{gspo} = 1.038pF, \quad C_{gdpo} = 291.9fF \]
\[ W_n = 1\mu, \quad L_n = 45n, \quad V_{tno} = +0.5V, \quad C_{bdn} = 5.156fF, \quad C_{gsno} = 1.947pF, \quad C_{gdno} = 135.8fF \]
The transistors are modeled with the following parameters:

\[ W_p = 1\mu, \quad L_p = 45n, \quad V_{t_p} = -0.5V, \quad C_{b_d p} = 2.293fF, \quad C_{g_s p} = 1.038pF, \quad C_{g_d p} = 291.9fF \]
\[ W_n = 1\mu, \quad L_n = 45n, \quad V_{t_n} = +0.5V, \quad C_{b_d n} = 5.156fF, \quad C_{g_s n} = 1.947pF, \quad C_{g_d n} = 135.8fF \]
BiCMOS implementation of the NAND function

Waveforms for the NAND function

The transistors are modeled with the following parameters:

$W_p=1\mu, L_p=45n, V_{tpo}=-0.5V, C_{bdp}=2.293fF, C_{gspo}=1.038pF, C_{gdpo}=291.9fF$

$W_n=1\mu, L_n=45n, V_{tno}=+0.5V, C_{bdn}=5.156fF, C_{gsno}=1.947pF, C_{gdno}=135.8fF$